# **IEEE 488/GPIB BUS INTERFACES**

## **DESCRIPTION**

The Model 4823B GPIB <-> Digital Interface Board is an IEEE-488.2/GPIB to digital interface with 56 I/O lines that can be used to easily adapt devices with digital signals to the IEEE-488/ GPIB/HP-IP bus. In a typical application, the 4823B is located inside the device chassis and is powered by the device's +5 volt power. All digital signal connections are on a 96-pin right-angle DIN connector at one end of the card. A 26-pin header on the other end of the 4823B contains the GPIB Bus and address switch input signals. The header connects to a companion GPIB Connector / Address Switch Board that mounts a GPIB Connector and Address Switch on the rear panel of the chassis.

4823B boards are also available with optional vertical and circuit-side DIN connectors to facilitate piggybacking the 4823B on a larger PC board. The 4823B's pinouts match the first 56 pins of ICS's earlier 4823A card so that the 4823B can be used as a replacement for the 4823A in applications that use no more than 56 I/O lines.

#### Versatile Digital Interface

The 4823B's digital interface is user configured with commands from the GPIB Bus. The configuration commands permit the user to designate the data lines as inputs and/or outputs in 8-bit byte increments, to connect the bytes into strings, set data polarity, data format, handshake modes and data format. When done, the setup configuration is saved in the 4823B's Flash memory and becomes the new power-on configuration. At power turn-on, the Digital I/O lines are initially tristated and then configured after self test.



4823B Interface Card

#### **Data Transfer Methods**

Data transfer between the GPIB bus and the 4823B's digital interface can be to or from specific bytes or as strings of values to or from one or more bytes. String transfers can be done with data transfer commands or transparently without commands. Binary output mode transfers data at rates > 50 Kbytes/sec. New bit operation commands set/reset specific bits in a byte and query a bit's status.

#### **Outputting Data**

Output byte commands latch an output value into a specific byte. Bit set/reset commands operate on a specific bit. Data Strobes can be manually generated if needed. Multiple output bytes can be outputted with a source data command or transparently without a command. The 4823B converts the data string into packed HEX bytes, latches the data in the configured output bytes and generates a data strobe pulse to update the external device. The data strings can be a series of decimal values, ACSII HEX characters, or the 30-3F HEX characters used in

# 4823B

# GPIB ← PARALLEL DIGITAL INTERFACE

A flexible interface between the IEEE 488 Bus and devices with digital signals.

- Provides a user-definable, 56-line parallel interface with bit, byte, string and binary data transfer capabilities.
   Fully configurable to the user's needs by bus commands.
- Signal monitor feature allows the 4823B to detect signal changes on 15 inputs.
   Relieves controller of time consuming polling function.
- High-current drivers and input pullup resistors.
   Drives more devices, longer lines and inputs CMOS signals or switch contacts.
- Device configuration, user's IDN message and bus address stored in Flash. Stored setup eliminates program initialization statements.
- Lock feature prevents accidental loss or change of user configuration.
   Protects your configuration and IDN message.
- Packaged on 3U VME size card with 4823A pinouts.
   Can be used to replace 4823A cards in 56 line applications.
- Includes a menu-driven configuration program.
   Steps user through configuration choices.

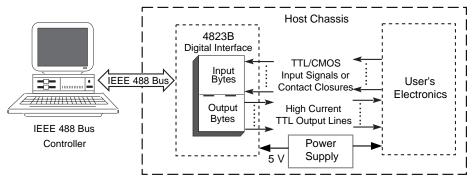


Figure 1 A typical 4823B Application



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ICS's 4823A series interfaces. Binary data transfers use the transparent output mode to transfer data bytes directly to the configured output bytes.

# **Reading Input Signals**

Input byte read commands read data from a specific byte. Bit read commands read a specific bit. Multiple input bytes can be read as strings with a data sense command or read transparently. For input strings, the 4823B reads the configured input bytes, converts the data to the selected output format, and outputs the data as a string of characters. Data can be inputted with or without handshaking. The input data can be formatted as decimal numbers, as ASCII HEX characters, or into a user selected character set.

# **Input Signal Monitoring**

The 4823B can monitor up to fifteen of the digital inputs for signal changes and generate an SRQ to notify the Bus Controller when changes occur. Monitoring is done by setting the 4823B's Questionable Transition register to detect positive and / or negative signal transitions and enabling bits in the Questionable Event register. When the enabled bit(s) are detected, the 4823B generates an SRQ to alert the Bus Controller to the event. The user queries the 4823B's Questionable Condition Register to determine the input signal states and the Event Register to learn which signal changed state. Application Bulletin 48-18 describes how to configure the 4823B's Status Reporting Structure registers and includes a program example.

# Configuring the 4823B

Figure 2 shows the 4823B's configuration and data transfer commands as a SCPI Command Tree. Each SCPI command has a corresponding Short Form command for quick programming. Most of the functions can also be queried to verify the command setting. (i.e. N? reads back talk byte selection)

The SYSTem branch sets the unit's GPIB address and addressing mode. The external address is for OEM boards.

The CONFigure branch assigns the bytes for string data transfer and sets their data polarity and handshaking. The CONFigure branch also sets the control signal polarities.

The FORMat branch sets the data conversion method and the characters in the user's Talk conversion table.

The new ROUTe branch gives the user a way to directly set and reset specific bits in a byte without the need to save a copy of the byte in his program.

The SENSe branch gives the user a way to read digital data from a single byte or from the configured input bytes. When reading data from a specific byte, input data polarity can be assigned on a bit-by-bit basis.

The SOURce branch provides a way to write values to a byte or to the configured output bytes. When data is outputted to a specific byte, output data polarity can be assigned on a bit-bybit basis.

The STATus branch (not shown) is used to setup and query the Operational and Questionable registers so that changes in the digital inputs or status inputs can be used to generate 488 Service Requests (SRQs). The Questionable registers can be

#### **4823B SCPI COMMAND TREE**

SCPI Commands	Short Form Cmds		
SYSTem :COMM :GPIB	GPIB Settings		
:ADDRESS :EXT	<numeric></numeric>		
:MODE :MONITOR :ERRor? :VERSion?	SINGle   DUAL   SEC <boolean></boolean>		
CONFigure [:DIGital]	Configure I/O		
:INPut :POLarity :HANDshake :OUTput :POLarity :HANDshake :CLEar :EDR :INHibit :REMote :RESet :STRobe :TRIGger :ASTATus :BSTATus	<channel list=""> 0   1 <boolean> <channel list=""> 0   1 <boolean> 0   1 <boolean> 0   1 0   1 0   1 0   1 0   1 0   1 0   1 0   1 0   1 0   1 0   1 0   1 0   1 0   1 0   1</boolean></boolean></channel></boolean></channel>	N TPn TBn LN LPn LH C E I R X S TR A B	
FORmat :TALK :TRANSlation :LISTen	<ascii hex="" hexl="" table=""  =""> &lt;16 char string&gt; <ascii 4833="" bin="" hex="" hexl=""  =""></ascii></ascii>	V	
ROUTe :CLOSe :OPEN :RESET	Bit Commands byte, bit byte, bit byte	CLOSE OPEN BRESET	
SENSe [:DIGital]	Input Data		
:DATA :DATA [:VALue]? :PORT? :PORTn? :POLarity? :RESet:EDR	number or <channel list=""></channel>	PI? BI? BIn? IPn ER	
:BIT? :BYTe?	0-1 0-255	READ? BREAD?	
[SOURce] [:DIGital]	Output Data		
:DATA [:VALue] :PORTn :POLarity :STRobe	0-255 0-255 0-255	PO BOn OPn SP	
CALibrate :IDN :DATe :DEFault	Calibrate Configuration string (72 char max) mm/dd/yy		
:DEFault :LOCK	1(On)  0(Off) [0]		

Figure 2 4823B SCPI Command Tree

used to monitor and query the first 15 digital I/O lines. The Operational registers can be used to examine or monitor the two external Status inputs.

The CALibrate branch provides a way to customize the 4823B with the user's own IDN message and to lockout the configuration parameters from being changed by the end user. The DEFault command restores the 4823B to ICS's factory defaults.

#### **4823B Connections**

The 4823B has two connectors for the Digital interface and for the GPIB signals and Address inputs.

Connector J1 is a 96-pin right-angle male DIN connector that contains the 4823B's digital I/O and power signals. The 4823B's pinouts are the same as the first 56 lines of ICS's older 4823A Interface Card. Mating DIN connectors are available with solder eyelet, wirewrap or solder pins. 4823B boards are also available with a male DIN connector mounted vertically on the component side or with a female DIN connector mounted vertically downwards on the circuit side of the board so the 4823B can be piggybacked on a larger PCB assembly.

Connector J2 is a 26-pin header that contains the 4823B's GPIB bus and external address switch input signals. When the external address function is enabled, the 4823B uses these signals to read its GPIB address from the rocker switch at power-on time. Connector J1 mates with ICS's GPIB Connector/Address Switch Board Assemblies. The Connector / Address Switch Assemblies are small, business card size PC assemblies that mount a GPIB connector and an 8-bit Address rocker switch to the rear panel of a chassis. The assemblies have a flat ribbon cable which plugs into the header on the 4823B. The assemblies are available in two layout styles. Refer to the separate data sheet for the GPIB Connector/Address Switch styles, mounting dimensions and cable lengths.

# **GPIB Address Modes**

The 4823B has three GPIB address modes: a single primary address, dual primary addresses or a primary address with secondary addresses 0 and 1. The single primary address and the lower address in either dual mode, is used for all commands, queries and for transferring data to and from the digital interface with the data commands. The upper GPIB address is used to transparently transfer data between the GPIB bus and the configured input or output bytes in the 4823B's digital interface.

# **Binary Data Transfer**

The binary data transfer mode can be

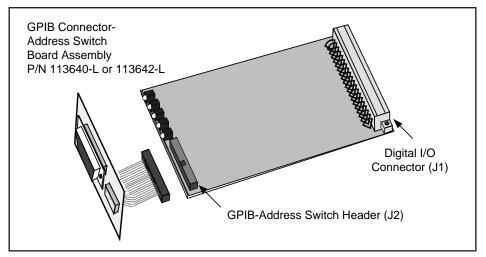


Figure 4 4823B Connection Method

used to quickly output large blocks of data to test devices or to load signal generators. The user configures the desired output bytes, sets the listen format to binary and enables a dual address mode. The 4823B is then addressed at its upper GPIB address and the binary data is outputted to the 4823B. The 4823B latches each bus character in a separate output byte and then pulses the data strobe when all bytes have been loaded. This sequence repeats until all of the binary data has been transferred.

# **4823A Replacement Concerns**

The 4823B can be used as a pin-to-pin replacement for ICS's earlier 4823A if the following concerns are addressed:

- 1. The 4823A application used only the first 56 I/O lines.
- 2. The 4823A split inputs and outputs on 4-bit nibble boundaries while the 4823B splits the inputs and outputs on 8-bit byte boundaries.
- 3. The 4823A only did transparent data transfers so driver routines or test programs may need some alteration to work with 4823B's string transfer
  - commands or with the 4823B's dual address modes if transparent data transfer is desired.
- Digital I/O lines should not be tied to each other unless connected with a 470 ohm or larger resistor.

#### 4823B Starter Kit

A 4823B Starter Kit is available for the first time GPIB user.

The Starter Kit includes a 4823B Board, a GPIB Connector/Switch Board Assembly, mating DIN connectors, a GPIB bus cable, a 488-PCIIt GPIB PCI card or a USB GPIB Controller for the PC, 488.2 Drivers and software. The software package includes a keyboard command line program, a Visual Basic configuration program and example programs. Limit of one Starter Kit per customer.

#### **OEM Customization**

OEM customization can be as simple as presetting the 4823B's I/O configuration and replacing ICS's IDN message prior to shipping or more complex by adding special SCPI commands and functions to the 4823B's firmware. A Sofware Development Kit ia available for OEMs who want to modify the 4823B's firmware.

OEMs who do not need multiple copies of the instruction manual and the configuration CD can buy just the 4823B board. Board only part numbers are shown in the Ordering Guide on the next page.

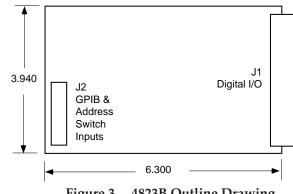


Figure 3 4823B Outline Drawing

#### **IEEE 488 Bus Interface**

The 4823B's 488 Bus interface meets IEEE STD 488.1-1987 and has the following capabilities:

SH1, AH1, T6, L4, SR1, PP0, DC1, RL0, DT1, C0 and E2 drivers.

# **Address Capability**

Dual primary addresses or single primary with secondary addresses 0 and 1. Primary address range: 0-30.

#### **SRO** Generation

SRQs are generated if the unit is not a talker, if SRQs are enabled and if an Enabled Event Status Register bit or if a monitored digital input change occurs. Digital inputs monitored by the Questionable registers.

#### 488.2 Common Commands

\*CLS, \*ESE, \*ESE?, \*ESR?, \*IDN?, \*OPC, \*OPC?, \*RCL, \*RST, \*SAV, \*SRE, \*SRE?, \*STB, TST? and \*WAI

#### **SCPI Commands**

Used to set and query all programmable functions. The 4823B conforms to SCPI 1994.0 Specification.

# Table 2 Programmable Functions

**GPIB Bus Address** Address mode Input Bytes Input Signal polarity Input Handshaking Talk data format Talk data conversion table **Output Bytes Output Polarity** Output Handshaking Listen data format Control line polarities SENSe input polarities SOURce output polarities STATus register configurations

# Signal Characteristics

The 4823B's parallel I/O signals have the following electrical characteristics. All time delays listed here are maximums, all pulse widths are minimums.

Inputs 56 Digital I/O,

2 Status and Reset Inputs Input High =  $> +2.0 \text{ V } @ \pm 10 \text{ } \mu\text{A}$ Logic  $Low = <0.8 \text{ V } @ 250 \ \mu\text{A}$ 

Levels with 33 Kohm pullup to +5 Vdc for sensing contacts.

Max high = 5.5 V

External Data Inhibit line Input Timing

SETS within 1 µs of the active edge of the EDR Input signal and resets after data is loaded. Data loading time for 6 BCD/ HEX characters is 0.15 ms (typ.) after the 4823B has been addressed as a Talker

Output High = >3 V with 3 mA source

Logic High =>2 V with 24 mA source Levels Low = 0.0 to +0.55 Vdc, 48 mA

Output Data is transferred to the Timing

output 0.6 to 5.3 ms after receipt of a terminator depending upon

transfer method.

**Data Stb** Output pulse width, 5 µs **Trigger** Output pulse width, 5 µs

**Remote** Output level asserted when in

the remote state

Reset Output pulse width, 40 µs for

\*RST command and true during 4823B reset time (70 ms)

# **Reset Inputs**

The 4823B is reset by a low going pulse on the External Reset input line or by pressing a miniature push-button on front edge of the 4823B's PCB

# **Diagnostic Indicators**

Six on board LEDs

PWR On when power applied On when self test passed **RDY** TALK On when addressed to talk LSTN On when addressed to listen SRO On when asserting SRQ line **ERR** On when ESR error bits set

#### **Physical**

Size, L x W x H 160 x 100 x 15 mm

(6.3 x 3.94 x 0.60 inches)

# **Connector and Headers**

GPIB/Addr: 26-pin 3M 2526 male conn. Digital I/O: 96-pin, 3 row male DIN conn

**Temperature** 

Operation -10° C to +70° C Storage -20° C to +85° C

Humidity

0-90% RH without condensation

Power +5 Vdc @ 400 mA (typical)

#### **Included Accessories**

Instruction Manual Configuration CD with sample programs

# **Available Accessories**

GPIB Connector / Addr Sw Assy with flat ribbon cable, 90 cm max., P/N 113640-90 or 113642-90. See GPIB Connector/Switch data sheet.

Mating DIN Connectors:

P/N 902023 Dolder Eyelet P/N 902024 Wirewrap P/N 902025 Dip Solder P/N 902058 Male Dip Solder

ORDERING GUIDE **Part Number** 

IEEE 488.2 to Parallel Digital Interface Board (Includes Instruction Manual and Configuration CD)	
IEEE 488.2 to Parallel Digital Interface Board (Board only)	
IEEE 488.2 to Parallel Digital Interface Board with vertical connector, Manual and Configuration CD	
IEEE 488.2 to Parallel Digital Interface Board with vertical connector (Board only)	
IEEE 488.2 to Parallel Digital Interface Board with circuit side connector, Manual and Configuration CD	
IEEE 488.2 to Parallel Digital Interface Board with circuit side connector (Board only)	
4823B Starter Package with 4823B, 488-PCIlt, Bus Cable, GPIB Connector/Switch Bd, and Connectors	
4823B Starter Package with 4823B, 488-USB, Bus Cable, GPIB Connector/Switch Bd, and Connectors	
GPIB Connector/Address Switch Assemblies and Mating Connectors  See separate	e data sheets